OIPE JC154
JAN 07 2005
PATENT & TRADEMARK OFFICE

FIG. 1 PRIOR ART

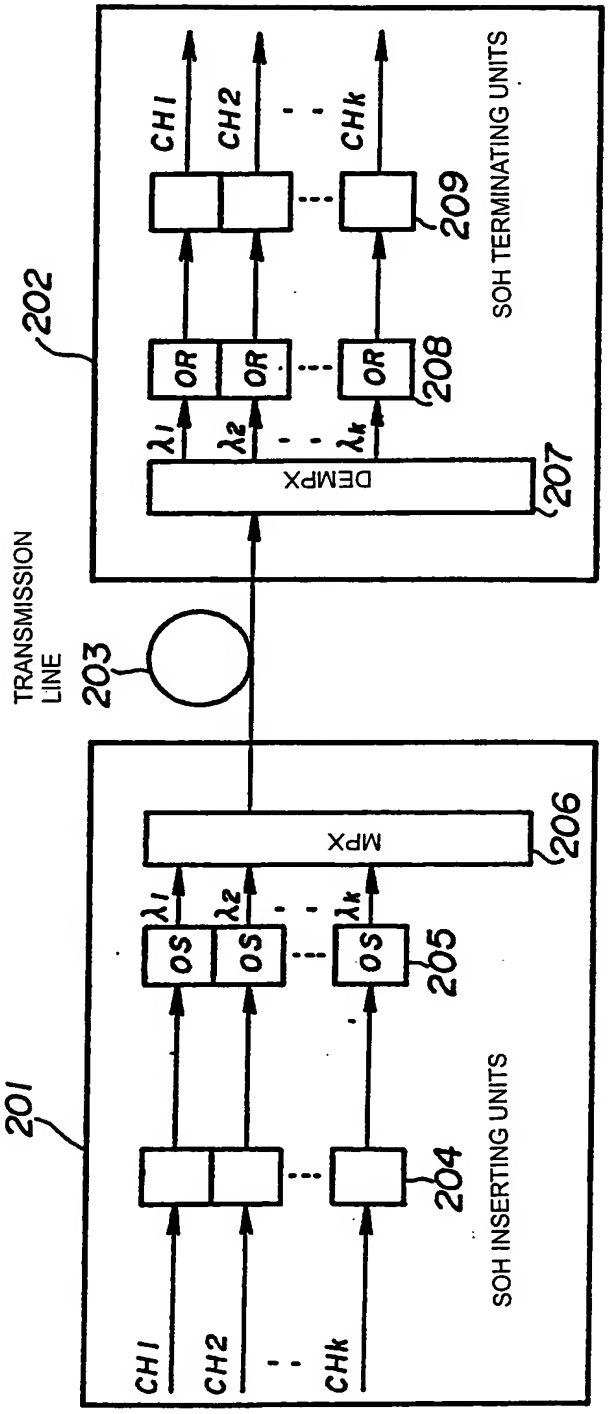


FIG. 2

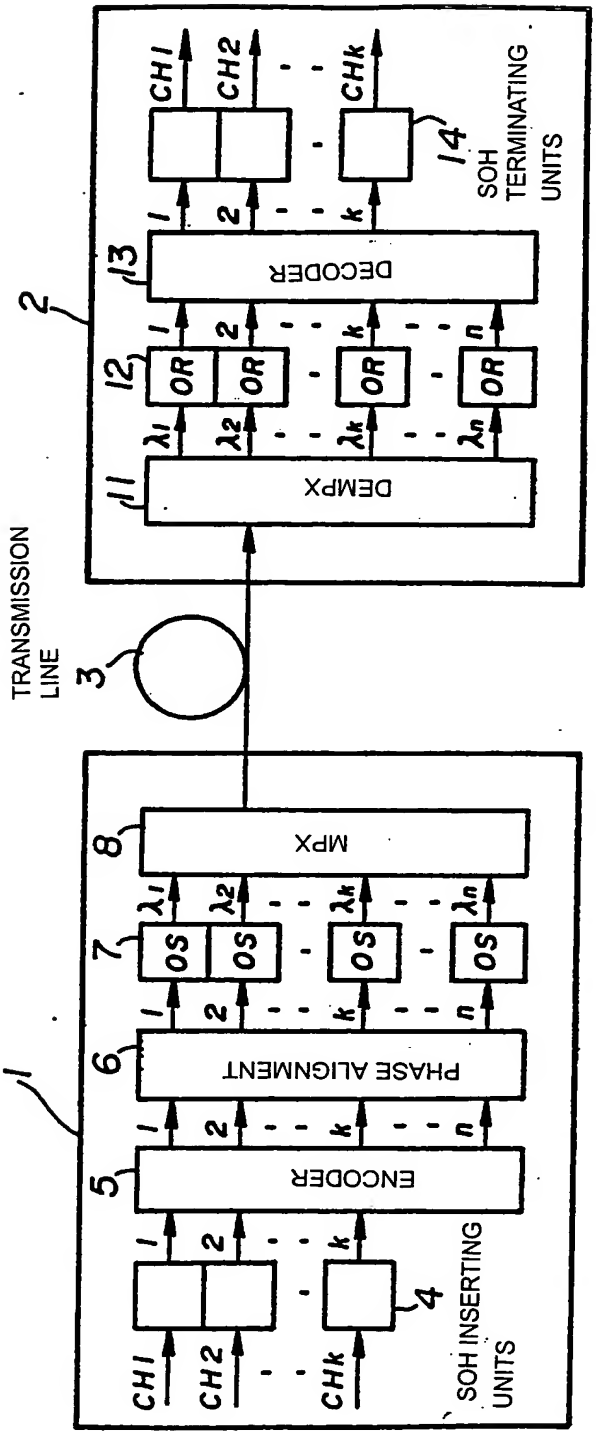

CH1
CH2
CHk
SOH INSERTING UNITS
4
ENCODER
5
PHASE ALIGNMENT
6
OS
7
MPX
8
TRANSMISSION LINE
3
DEMPX
11
OR
12
DECODER
13
SOH TERMINATING UNITS
14
1
2

FIG.3

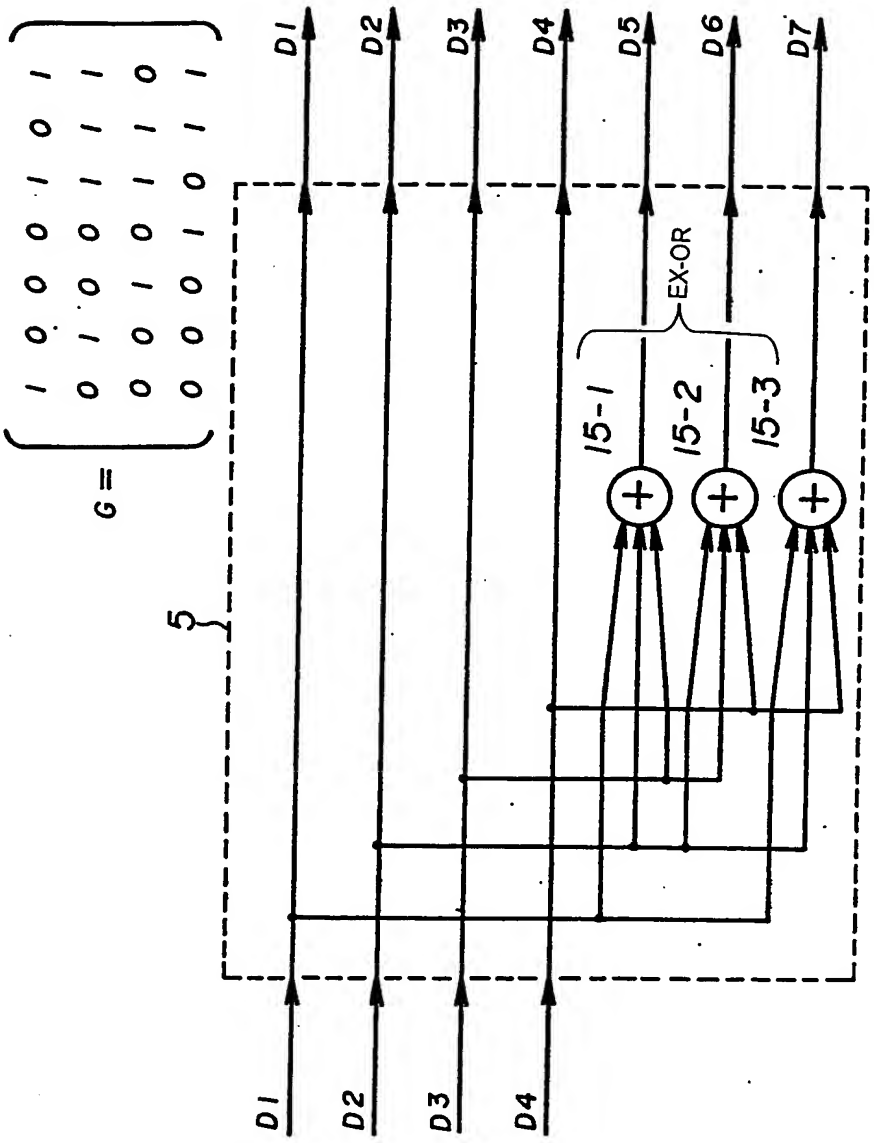

G =
1 0 0 0 0 1 0 1
0 1 0 0 1 1 1 1
0 0 1 0 1 1 1 0
0 0 0 1 0 1 1 1
5
D1
D2
D3
D4
D5
D6
D7
EX-OR
15-1
15-2
15-3
D1
D2
D3
D4

FIG.4

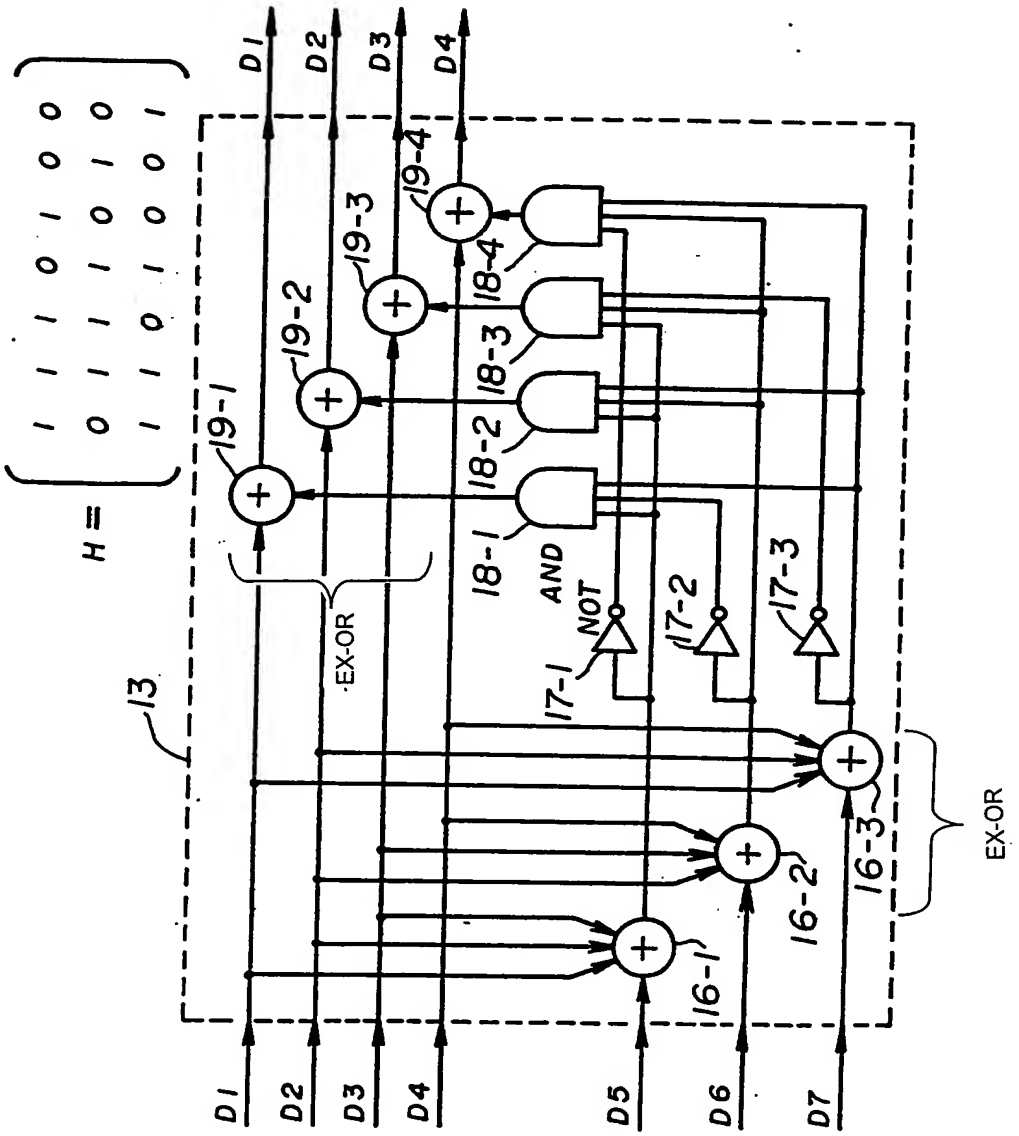

H =
1 1 1 0 1 0 0
0 1 1 1 0 1 0
1 1 0 1 0 0 1
D1
D2
D3
D4
D5
D6
D7
13
19-1
19-2
19-3
19-4
18-1
18-2
18-3
18-4
17-1
17-2
17-3
16-1
16-2
16-3
AND
NOT
EX-OR
EX-OR

FIG. 5

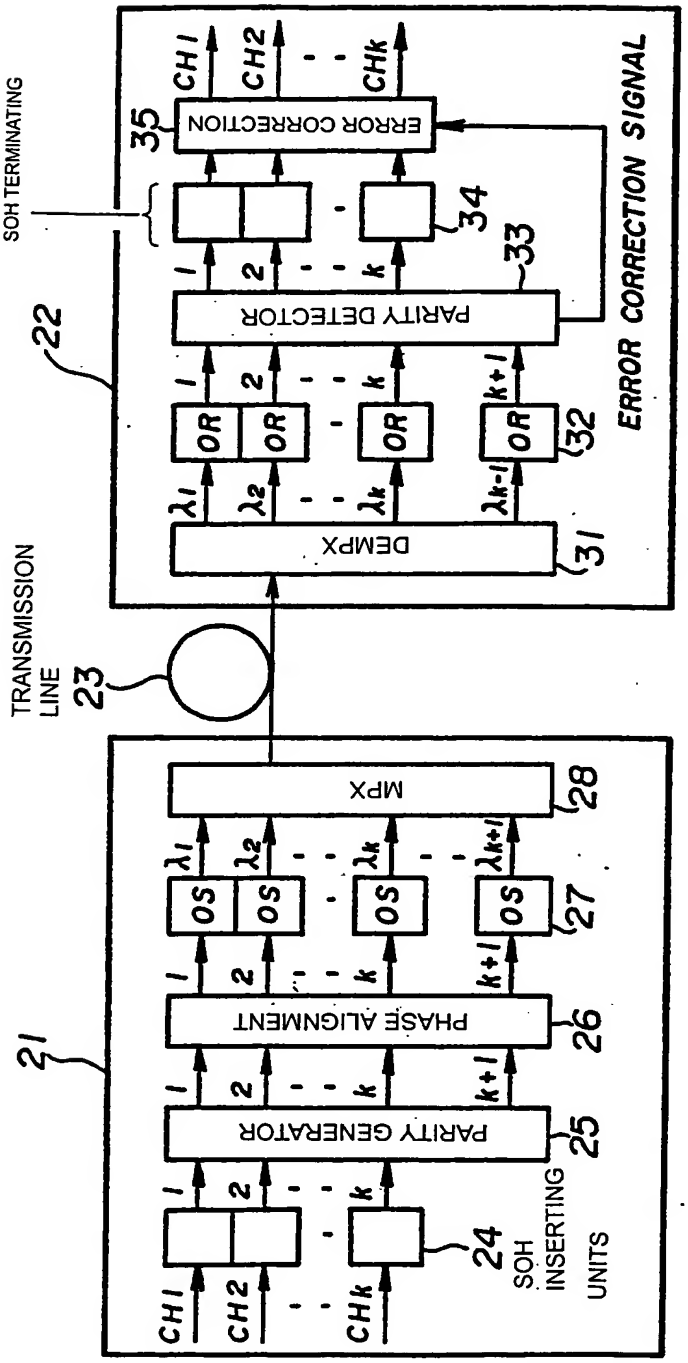

SOH TERMINATING
TRANSMISSION LINE
23
22
21
ERROR CORRECTION SIGNAL
CH1
CH2
CHk
ERROR CORRECTION
35
34
33
PARITY DETECTOR
OR
32
DEMPX
31
MPX
28
OS
27
PHASE ALIGNMENT
26
PARITY GENERATOR
25
SOH INSERTING UNITS
24

FIG.6

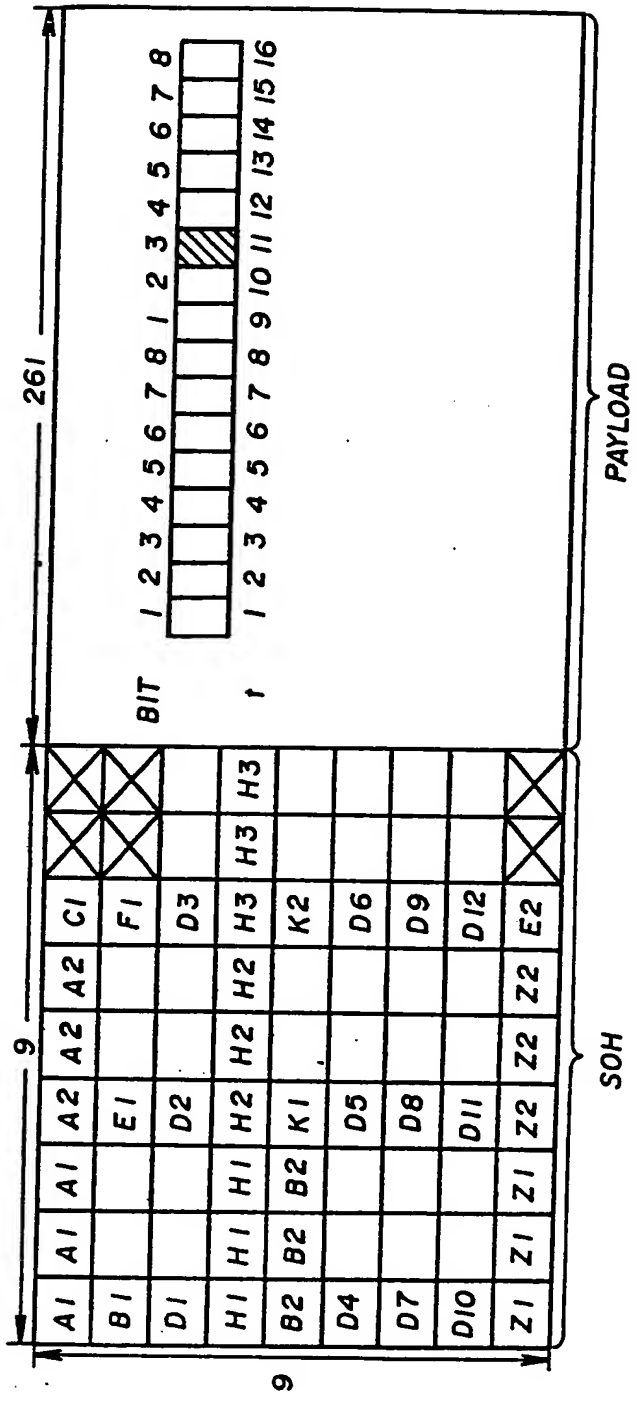

261
9
9
PAYLOAD
SOH
BIT
1 2 3 4 5 6 7 8
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
A1 A1 A2 A2 A2 C1 H3
B1 E1 F1 H3
D1 D2 D3 H2 K2 D6 D9 D12 E2
H1 H1 H2 H2 H2 Z2 Z2
B2 B2 K1 D5 D8 D11 Z2
H1 B2 D4 D7 D10 Z1
Z1 Z1 Z1

FIG. 7

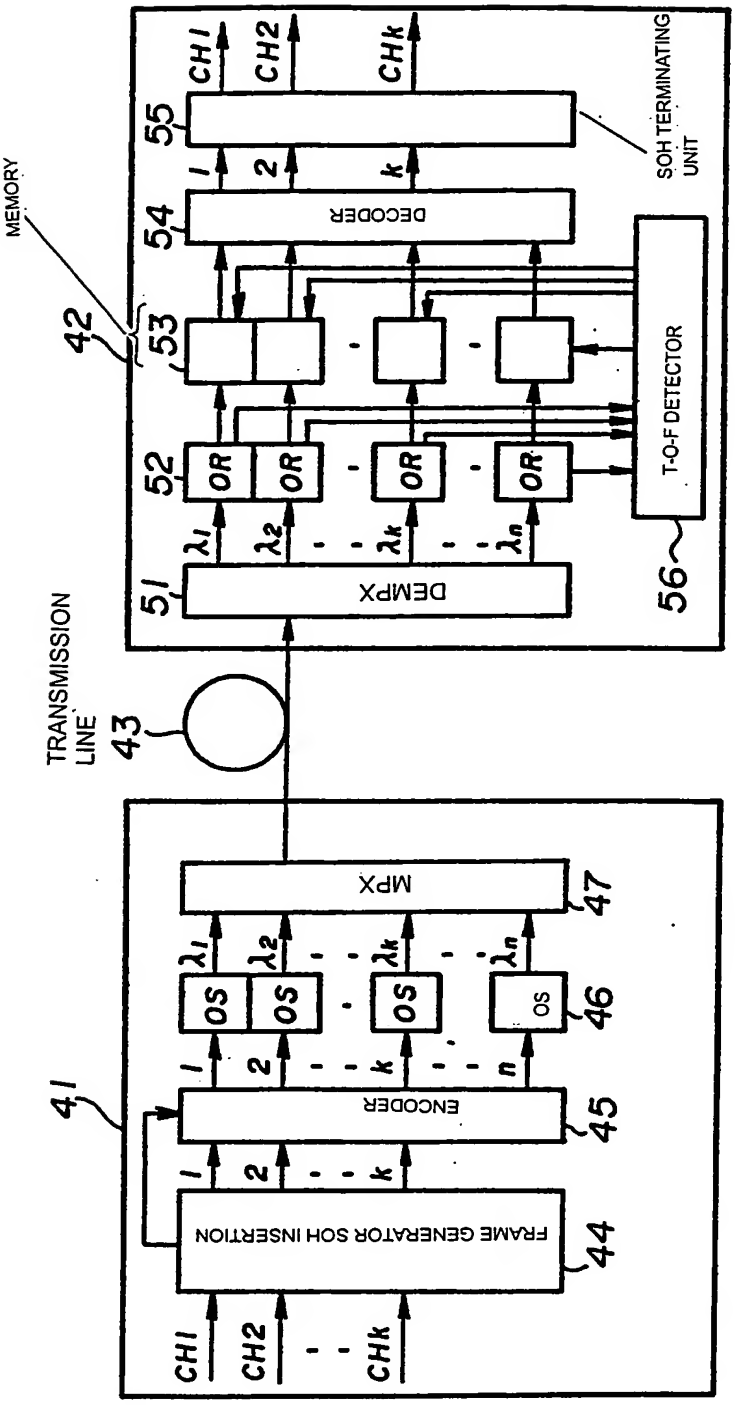

FRAME GENERATOR SOH INSERTION
ENCODER
MPX
OS
DEMPX
OR
DECODER
T-O-F DETECTOR
SOH TERMINATING UNIT
MEMORY
TRANSMISSION LINE
CH1
CH2
CHk
41
42
43
44
45
46
47
51
52
53
54
55
56

FIG. 8

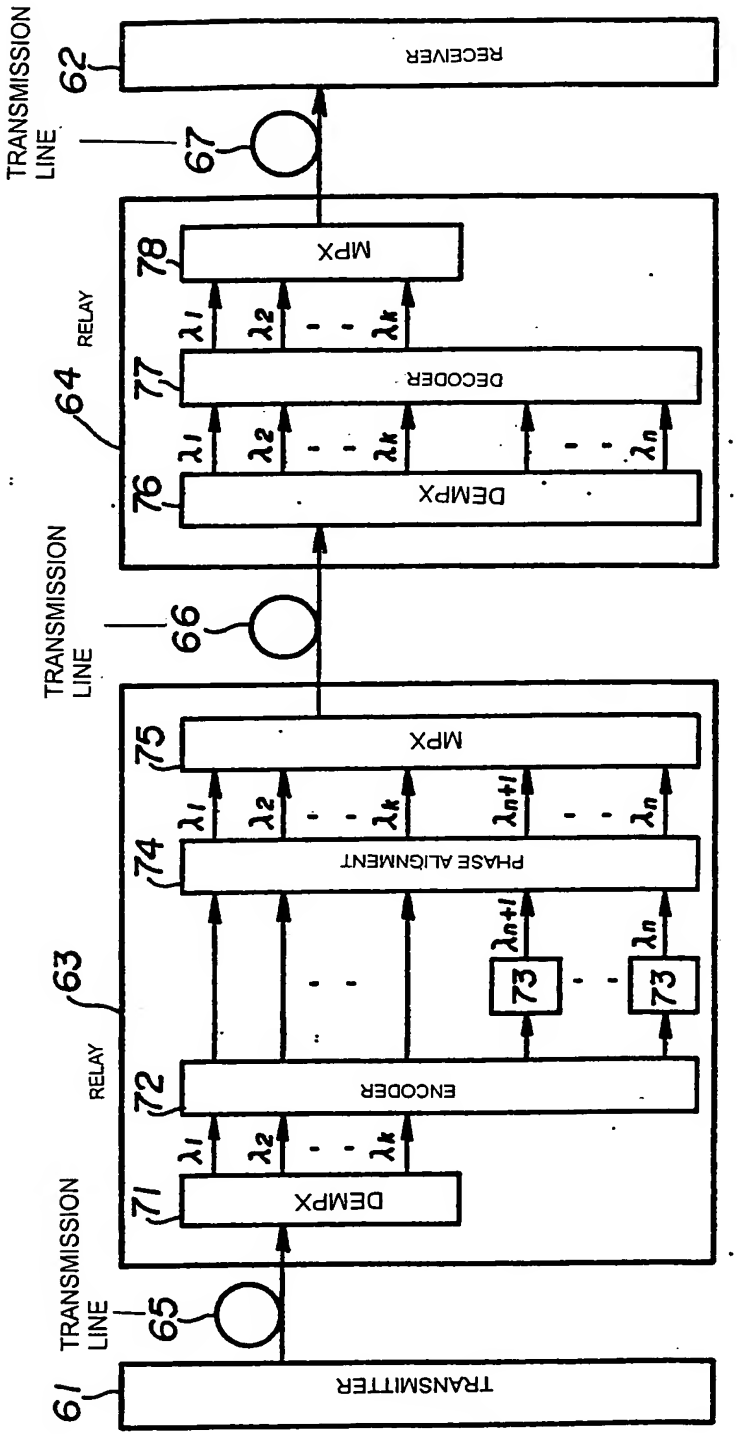

TRANSMITTER
61
TRANSMISSION LINE
65
DEMPX
71
RELAY
63
ENCODER
72
PHASE ALIGNMENT
74
MPX
75
TRANSMISSION LINE
66
DEMPX
76
RELAY
64
DECODER
77
MPX
78
TRANSMISSION LINE
67
RECEIVER
62
λ1
λ2
λk
λn
λn+1
73

FIG. 9

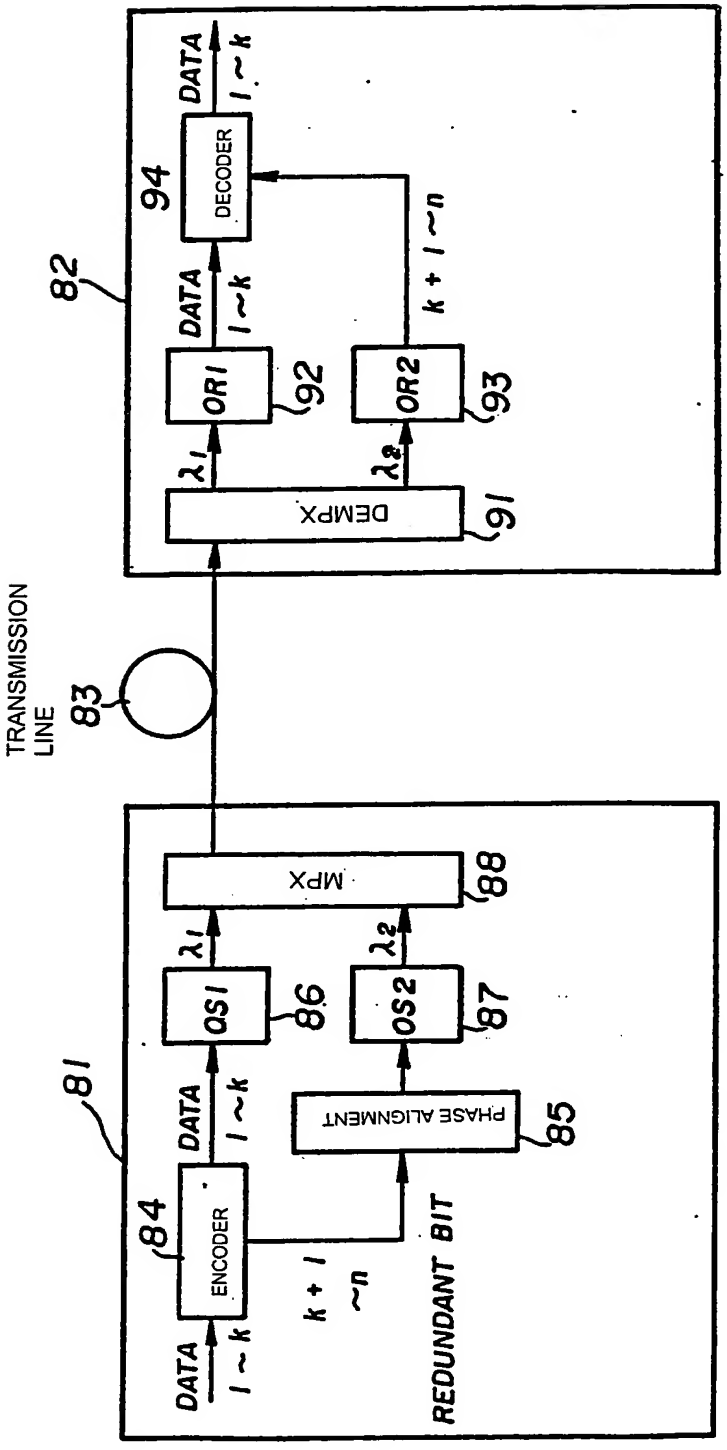

81
82
83
84
85
86
87
88
91
92
93
94
ENCODER
PHASE ALIGNMENT
OS1
OS2
MPX
DEMPX
OR1
OR2
DECODER
DATA
1 ~ k
k + 1 ~ n
REDUNDANT BIT
TRANSMISSION LINE
λ1
λ2

FIG. 10

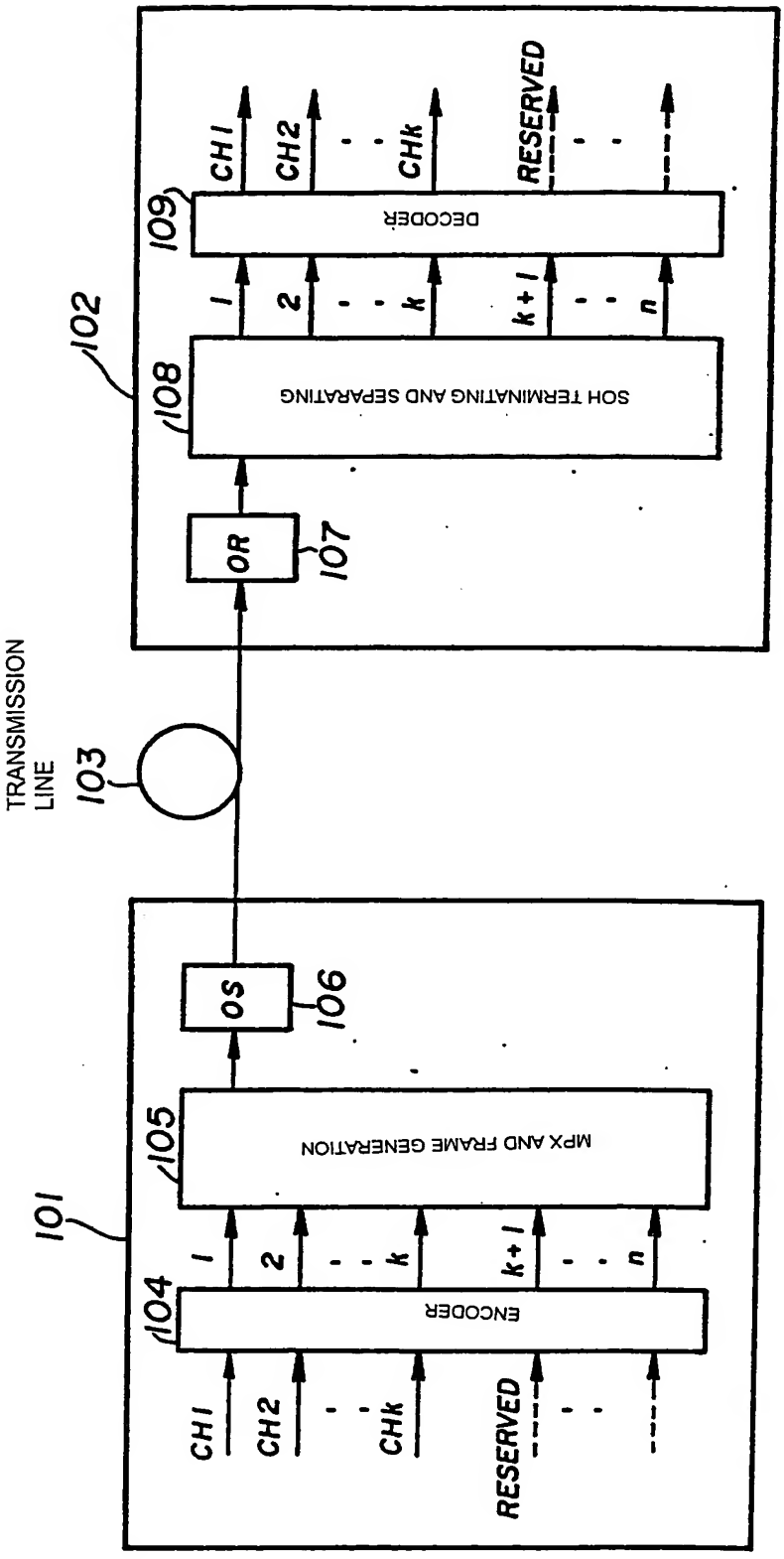

101
102
103
TRANSMISSION LINE
104
ENCODER
105
MPX AND FRAME GENERATION
106
OS
107
OR
108
SOH TERMINATING AND SEPARATING
109
DECODER
CH1
CH2
CHk
RESERVED
1
2
k
k+1
n

FIG. 11

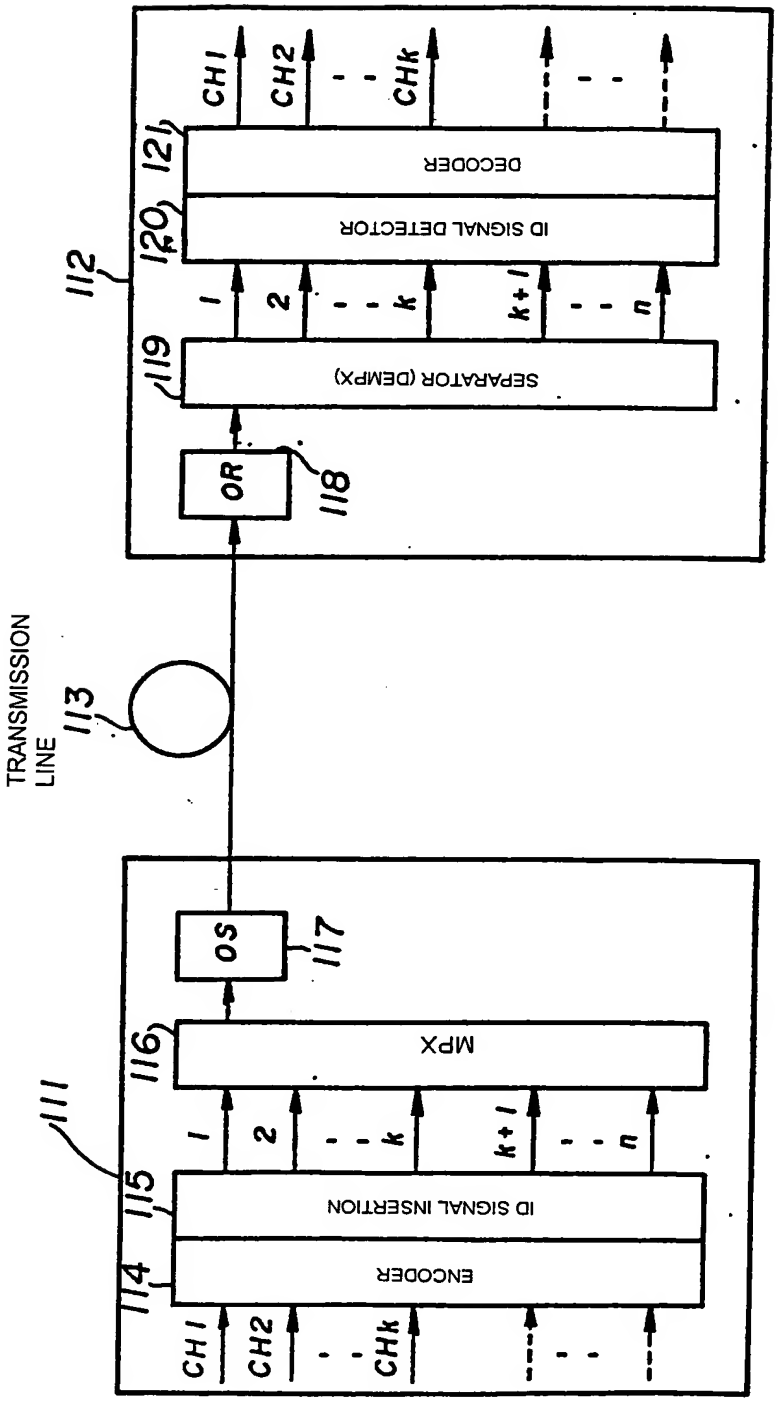

CH1
CH2
CHk
DECODER
ID SIGNAL DETECTOR
SEPARATOR (DEMPX)
OR
OS
MPX
ID SIGNAL INSERTION
ENCODER
TRANSMISSION LINE
111
112
113
114
115
116
117
118
119
120
121

FIG. 12

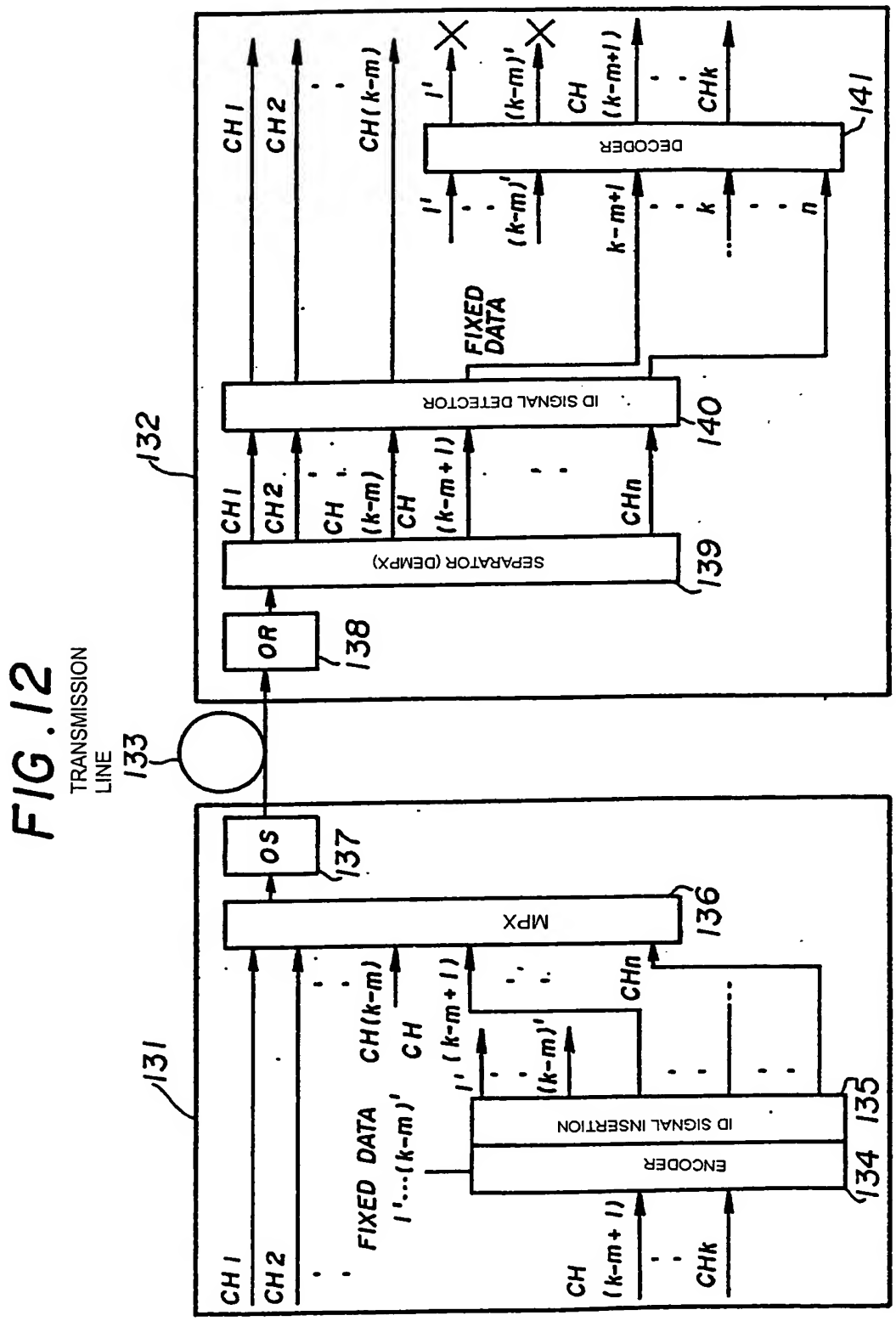
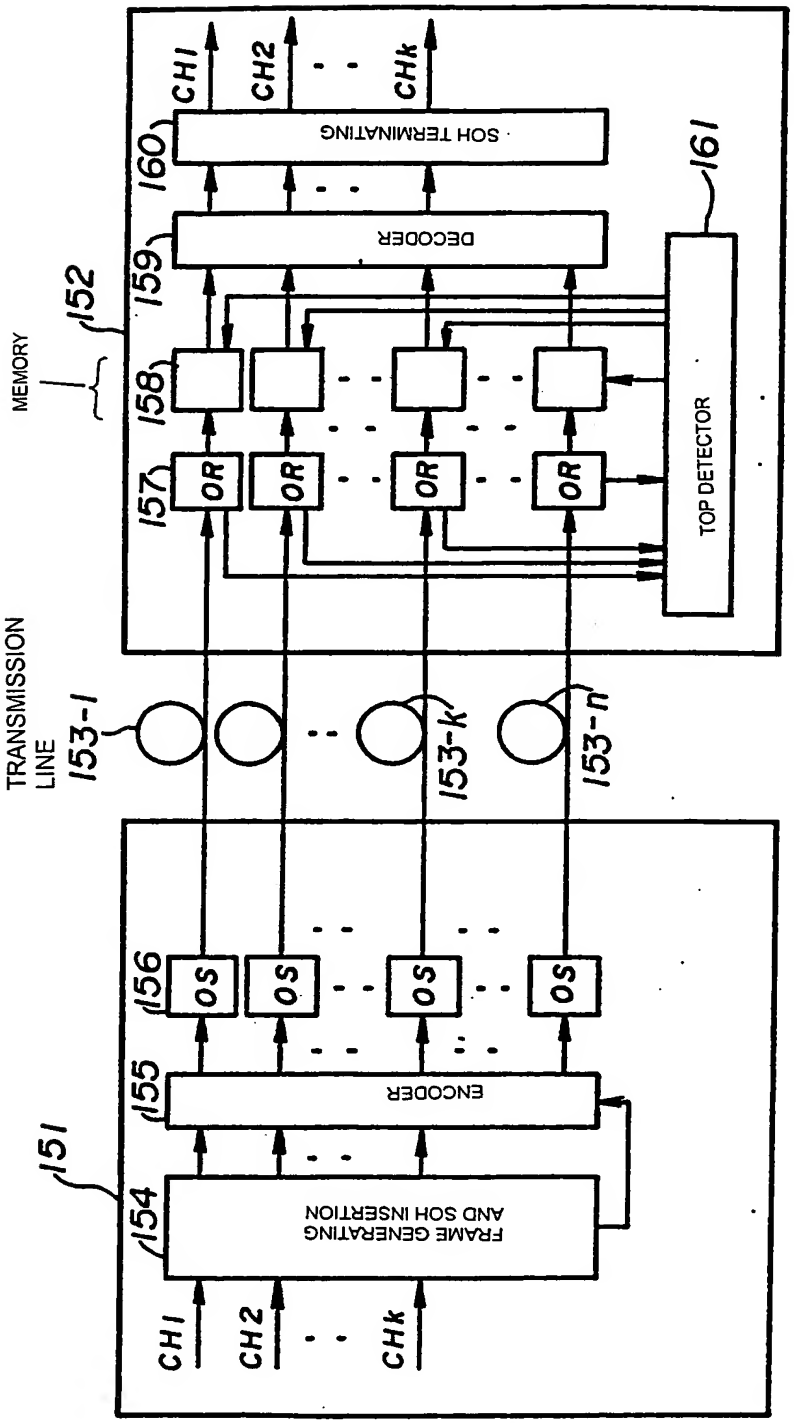

TRANSMISSION LINE
133
131
132
OS
137
MPX
136
ID SIGNAL INSERTION
ENCODER
134
135
OR
138
SEPARATOR (DEMPX)
139
ID SIGNAL DETECTOR
140
DECODER
141
CH1
CH2
CH(k-m)
CH (k-m+1)
CHn
CHk
FIXED DATA
1'...(k-m)'
1'
(k-m)'
k-m+1
k
n

FIG. 13


CH1
CH2
CHk
SOH TERMINATING
160
161
DECODER
159
152
MEMORY
158
157
OR
TOP DETECTOR
TRANSMISSION LINE
153-1
153-k
153-n
156
OS
155
ENCODER
151
154
FRAME GENERATING AND SOH INSERTION
CH1
CH2
CHk